PATENT
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MULTIPLY-ACCUMULATE MODULES AND PARALLEL MULTIPLIERS AND METHODS FOR DESIGNING MULTIPLY-ACCUMULATE MODULES AND PARALLEL MULTIPLIERS

ABSTRACT OF THE DISCLOSURE

A multiply-accumulate module (100) includes a multiply-accumulate core (120), which includes a plurality of Booth encoder cells (104a). The multiply-accumulate core (120) also includes a plurality of Booth decoder cells (110a) connected to at least one of the Booth encoder cells (104a) and a plurality of Wallace tree cells (112a) connected to at least one of the Booth decoder cells (110a). Moreover, at least one first Wallace tree cell (112a1) or at least one first Booth decoder cell (110a1), or any combination thereof, includes a first plurality of transistors, and at least one second Wallace tree cell (112a2) or at least one second Booth decoder cell (110a2), or any combination thereof, includes a second plurality of transistors. In addition, at least one critical path of the multiply-accumulate module (100) includes the at least one first cell and a width of at least one of the first plurality of transistors is greater than a width of at least one of the second plurality of transistors.